Amendments to the Claims

1. (currently amended) A quantum device, comprising:

~~a pair of dopant atoms located in~~ an ~~otherwise~~ electrically inert solid ~~substrate in which it is possible to ionise the dopant atoms; wherein the two dopants produce a double-well electric potential and a charge qubit is realised by the location of one or more electrons or holes within this potential~~ within which there is;

a charge qubit comprising a pair of dopant atoms having a net charge and an electric field having two potential wells, wherein the two potential wells are located adjacent respective dopant atoms;

and wherein the location of the net charge in the electric field having two potential wells defines the logical state of the qubit;

and wherein a first gate is located over a potential barrier between the two potential wells to control barrier height; and,

at least one second gate is located to control relative shapes and sizes of the two potential wells.

2. (currently amended) A quantum device according to claim 1, wherein the substrate is silicon, the dopant is phosphorus and the charge qubit is ~~ionisation of one of the donor electrons creates~~ a $P\text{-}P^+$ system and its electrical field having two potential wells.

3. (currently amended) A quantum device according to claim 2, wherein ~~a~~ the logical state of the charge qubit is ~~formed~~ defined by the location of a single electron in one ~~or other~~ of the two potential wells ~~of the double-well potential~~.

4. (currently amended) A quantum device according to claim 2, wherein the the logical state of the charge qubit is ~~formed~~ defined by ~~the~~ lowest symmetric or antisymmetric molecular states.

5. (currently amended) A quantum device according to claim 2, wherein ~~the~~ spacing between the P atoms is up to 200nm.

6. (original) A quantum device according to claim 5, wherein the spacing between the P atoms is in the range 20 to 100nm.

7. (currently amended) A quantum device according to claim 2, wherein the two P atoms are buried to a depth in the substrate up to 200nm ~~below the surface of the device~~.

8. (currently amended) A quantum device according to claim 7, wherein the two P atoms are buried to a depth in the substrate in the range 5 to 50nm.

9. (original) A quantum device according to claim 2, wherein the silicon substrate is coated with an insulating layer to isolate the donor electrons from any surface electrodes.

10. (original) A quantum device according to claim 9, wherein the insulating layer is SiO_2,

11. (currently amended) A quantum device according to claim 2, wherein gate electrodes are placed on the surface of the substrate above the donor atoms to allow for external control of ~~the~~ charge wavefunctions.

12. (currently amended) A quantum device according to claim 11, wherein ~~a~~ the first gate ~~is located over the potential barrier, between the two wells, to control the barrier height, this gate~~ is known as the `barrier' gate or B-gate.

13. (currently amended) A quantum device according to claim 12, wherein ~~a~~ the at least one second gate~~, or more than one second gate, is provided to control the relative shapes and sizes of the two wells, this gate~~ is known as the >potential off-set=, >symmetry= or S-gate.

14. (original) A quantum device according to claim 13, wherein suitable biasing of the first and second gates allows one qubit logic operations to be performed.

15. (original) A quantum device according to claim 11, wherein one or more charge detection devices are provided on the surface of the substrate for qubit readout and to confirm initialization of qubits.

16. (original) A quantum device according to claim 15, wherein the charge detection device is a sensitive field-effect transistor, or a single electron transistor (SET).

17. (currently amended) A quantum device according to claim 2, ~~wherein the configuration~~ comprising two dopant atoms, surface gates and surface charge detection devices, ~~is~~ repeated many times on a single silicon chip, allowing for scale-up to a many qubit processor.

18. (currently amended) A quantum device according to claim 17, wherein the device is cooled to ensure that the donors are not thermally ionised and to minimise coupling of the charge qubits to an ~~the~~ environment.

19. (currently amended) A quantum device according to claim 18, wherein ~~it~~ the device is cooled to 4K or below.

20. (original) A quantum device comprising two pairs of dopant atoms, each located in a solid substrate such that two double-well potentials are created; and two charge qubits are formed by the location of one or more electrons within the double-well potentials; where, one or more gates above the substrate control electron tunneling between the two qubits; and where, by suitable biasing of these and other gate electrodes, two-qubit logic operations may be performed.

21. (original) A quantum device comprising two pairs of dopant atoms, each located in a solid substrate such that two double-well potentials are created; and two charge qubits are formed by the location of one or more electrons within the double-well potentials; and where, one or more gates above the substrate controls the Coulomb interaction between the two qubits; and where, by suitable biasing of these and other gate electrodes, two qubit logic operations may be performed.

22. (original) A quantum device comprising more than one of the devices comprising two pairs of donor atoms, arranged adjacent each other, and having gates to enable interaction between each adjacent pair.

23. (previously presented) A method of reading out the logic state of a qubit from a quantum device having a single electron transistor (SET) having an S-gate, comprising the steps of:

(i) Biasing the S-gate to a non-zero value to define a known relaxed state for which the SET has been previously calibrated;

(ii) Turning on the SET;

(iii) Waiting for a period of time for the system to relax to the relaxed state;

(iv) Monitoring SET current during the waiting period to determine whether a change of state occurs, or not;

(v) Inferring the state before step (i) from the behaviour of the SET current monitored during step (iv).

24. (previously presented) A method of initializating the logic state of each qubit in a quantum device having a single electron transistor having an S-gate, comprising the steps of:

(i) Biasing the S-gate to a non-zero value to define a known relaxed state;

(ii) Waiting for a period of time for the system to relax to the relaxed state.

25. (original) A method of using a quantum device according to any one of claims 1 to 22 to perform quantum computations, comprising typical steps which include:

(i) Initializing each qubit in the quantum device;

(ii) Using a suitable quantum algorithm to carry out one-qubit and two-qubit operations on the qubits in the device via an appropriately timed sequence of control gate biasing;

(iii) Reading out the logical states of the qubits.

26. (previously presented) A method of making a quantum device a quantum device, comprising the steps of:

(i) creating a resist mask for implantation of an array of one or more pairs of dopant atoms into a semiconductor substrate;

(ii) implanting one dopant ion through each hole in the mask to form an array of buried-atom qubits;

(iii) fabricating conducting electrodes above each implanted pair of donor atoms to serve as a B gate, an S gate and a SET;

(iv) annealing the device to a temperature sufficient to remove implant lattice damage and activate the dopant B this step may occur either immediately before or after step (iii);

(v) pre-initializing each pair of donor atoms to remove one of the electrons.

27. (previously presented) A method of making a quantum device, comprising the steps of:

(i) passivating a clean semiconductor surface;

(ii) patterning the passivated surface to open an array of holes;

(iii) exposing the resulting surface to donor atoms, perhaps in the form of dopant-bearing molecules;

(iv) overgrowing the dopant atom array with further layers of the semiconductor and annealing if necessary;

(v) coating the surface with an insulating layer if necessary;

(vi) fabricating conducting electrodes above each implanted pair of donor atoms to serve as a B gate, an S gate and a SET;

(vii) pre-initializing each pair of donor atoms to remove one of the electrons.